Characterization of BTI in SiC MOSFETs Using Third Quadrant Characteristics

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***Abstract*—Bias Temperature Instability (BTI) is a reliability concern for SiC MOSFETs which can have serious implications in the application if the true extent of the threshold voltage shift is underestimated. In this paper the third quadrant characteristics of SiC MOSFETs are used for characterizing the impact of accelerated gate stresses, evaluating the peak threshold voltage shift and tracking the recovery after stress removal. This method allows the evaluation of the impact of cumulative pulsed stresses of both long and short duration, which can be fundamental for characterizing the dynamics of BTI-induced threshold voltage shift in SiC MOSFETs under repetitive switching at the rated and accelerated gate voltage stresses.**

Keywords—Bias Temperature Instability, SiC MOSFET

I. Introduction

Despite the improvements of the new generation SiC power MOSFETs, Bias Temperature Instability remains a reliability concern hence application engineers using SiC MOSFETs should take threshold voltage (V_{TH}) shift into consideration. BTI is highly relevant to SiC MOSFETs due to a high density of oxide and interface traps at the SiC/SiO_2 interface, as well as small band offsets due to the wider bandgap [1-4]. A peculiar characteristic of BTI in SiC is the recovery of V_{TH} after stress removal. This recovery can mislead device engineers causing them to underestimate the true extent of the V_{TH} shift after High Temperature Gate Bias (HTGB) stress. In high current applications where parallel connected SiC MOSFETs can be biased at negative gate voltages for long standby periods, loss of gate synchronization due to non-uniform V_{TH} shift can cause electrothermal destruction from poor current sharing. The lack of recovery time after V_{GS} bias in the application makes the standard reliability tests that allow recovery time unsuitable. It is therefore necessary to devise techniques for evaluating the V_{TH} shift and recovery in real-time. This paper evaluates how a novel method for characterizing V_{TH} shift caused by BTI presented by the authors in [5] can be used for evaluating cumulative stress pulses and capture phenomena that are not apparent during the conventional long stresses for BTI characterization.

II. Bias Temperature Instability Overview And Experimental Setup

BTI in SiC MOSFETs is a topic of interest, given the recent number of publications [1-4]. Depending on the polarity of the stress, the shift of V_{TH} can be positive or negative, giving either Positive Bias Temperature Instability (PBTI) or Negative Bias Temperature Instability (NBTI). Fundamental for evaluating the impact of BTI in SiC MOSFETs is capturing the peak V_{TH} shift after the stress and the subsequent recovery once the stress is removed.

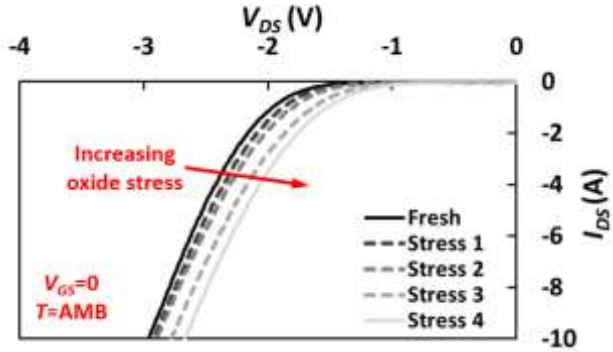

Fig. 1 Impact of NBTI on the 3rd quadrant characteristics of a SiC MOSFET. Cumulative negative HTGB stresses performed at 150 °C, as defined in [5]

To that end, different methods have been proposed [1, 3], since the erroneous determination of the V_{TH} shift can have negative consequences on the qualification of the devices. Using the methodology presented by the authors in [5], the peak shift and recovery of V_{TH} after the stress removal can be detected. The methodology is based on 3rd quadrant characteristics of SiC MOSFETs. The threshold voltage shift caused by BTI affects the value of the source-drain voltage V_{SD} when V_{GS} = 0 V**.** This is caused by the partial conduction of current through the channel when V_{GS}=0 known as the body effect in SiC MOSFETs. Fig. 1 shows the measured 3rd quadrant characteristics of a SiC planar MOSFET at ambient temperature which was subjected to highly accelerated negative HTGB stresses, using a high gate voltages at a temperature of 150 °C as defined in [5]. The 3rd quadrant characteristics were measured at ambient temperature, after 16 hours relaxation at V_{GS}=0, so as to characterize only the

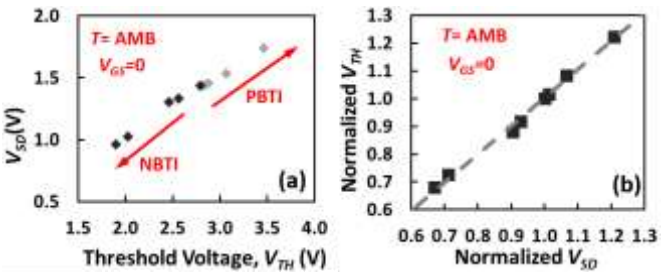

Fig. 2 (a) V_{SD} as a function of threshold voltage V_{TH} during both PBTI and NBTI, (b) Normalized V_{TH} as a function of the normalized V_{SD} (measured at I_{SD}=50 mA) (Stresses defined in [5])

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permanent V_{TH} shift caused by the stress.

Similar to the use of V_{SD} as Temperature Sensitive Electrical Parameter (TSEP), using both positive and negative stresses a relationship between V_{TH} and V_{SD} can been defined. This is shown for the evaluated planar SiC MOSFET in Fig. 2, for a defined temperature (ambient) and a low value sensing current I_{SENSE} of 50 mA (this is the current used to measure V_{SD} during 3rd quadrant operation). As V_{SD} is temperature dependent, it is important that I_{SENSE} does not cause the self-heating of the device hence a suitable cooling method to minimize the impact of temperature is required. The normalized values are used to define a relationship between V_{SD} and V_{TH}, given by (1) [5].

$$V_{TH,norm} = 1.02 \cdot V_{SD,norm} - 1.02 \quad (1)$$

The test setup used here is similar to the test setup used for determining the junction temperature using V_{SD} as TSEP [6] and it is shown in Fig. 3. It consists of a gate driving circuit used for stressing the gate oxide with a defined V_{GS} stress and a current source which injects the sensing current I_{SENSE} flowing from source to drain. The stress timing signal is generated using a waveform generator model TDS2024C from Tektronix, the transient V_{SD} is measured using a differential probe model TA-043 from Pico Technology and captured using an oscilloscope model TDS5054B from Tektronix. The sensing current I_{SENSE} is measured using a digital multimeter Fluke 175. Depending on the gate voltage used, I_{SENSE} will flow: (a) through the channel only (positive V_{GS} which fully turns ON the device), (b) through the parasitic body diode (sufficient negative V_{GS}) or (c) there is a current divider between the body diode and the MOSFET channel, due to the body effect and depending on V_{TH} (V_{GS}= 0 V). Using the calibration curve obtained in Fig. 2, for a known temperature the threshold voltage shift can be detected by measuring V_{SD}.

Fig 4 shows the application of this technique. In this figure, the V_{GS} stress (17 V) is shown in Fig. 4(a), together with the measured V_{SD} in Fig. 4(b) and the calculated normalized V_{TH} in Fig. 4(c) (equation (1) has been used for $V_{TH,norm}$ calculation). Before the application of V_{GS} (for t < 4 s), the measured V_{SD} is 1.4 V (corresponding to nominal V_{TH}). During V_{GS} stress application (4 s < t < 14 s), V_{SD} falls to the ON-state resistance since the MOSFET is ON. After the V_{GS} stress is removed (t > 14 s), V_{SD} increases to a 6% higher value corresponding to increased V_{TH} from PBTI due to negative charge trapping. Hence, the technique here shows

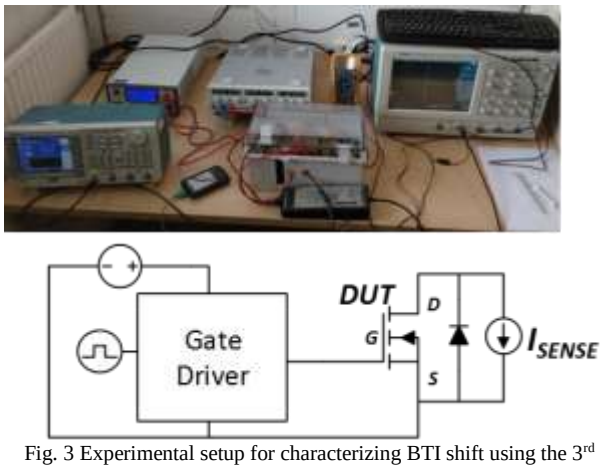

Fig. 3 Experimental setup for characterizing BTI shift using the 3rd quadrant characteristics of a SiC MOSFET

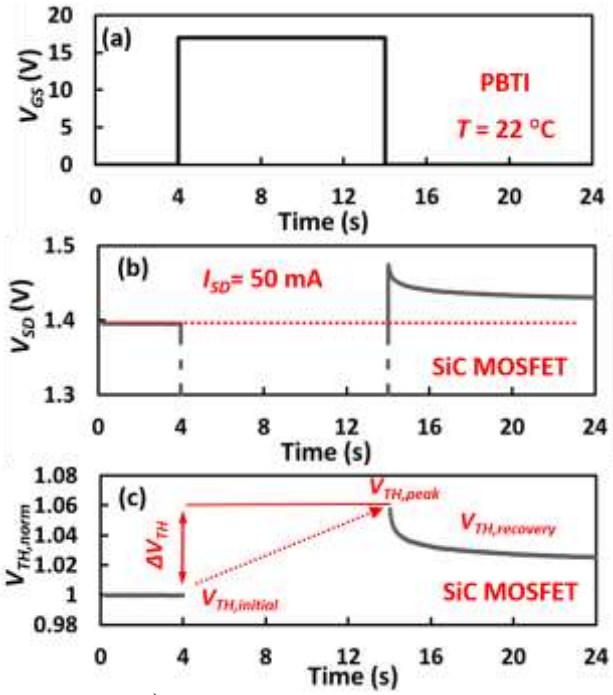

Fig. 4 Use of 3rd quadrant for BTI characterization: (a) Gate voltage stress, (b) 3rd quadrant V_{SD} voltage measured using I_{SD}= 50 mA, (c) Normalized V_{TH} pre and after stress

a 6 % increase in V_{TH} due to a 10 s application of the rated V_{GS}. More details of the measurement technique for NBTI and PBTI are available in [5].

III. Impact of Repetitive Gate Stress Pulses on BTI

In [5], the method was introduced and evaluated for short stress pulses. However, one of the main benefits of this method is that it enables the investigation of the impact of stress duration on BTI and V_{TH} recovery as well as the impact of repetitive stresses on the dynamics threshold voltage shift. Using the test setup presented in Fig. 3, both the impact of short and long repetitive stress pulses has been evaluated for the selected SiC MOSFET. This can be fundamental for understanding threshold voltage shift during the initial phases of a long stress.

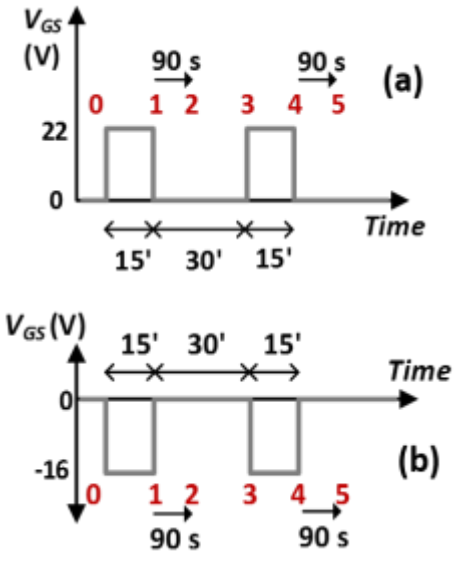

Fig.5 Long duration repetitive stress pulses for evaluation of: (a) PBTI and (b) NBTI

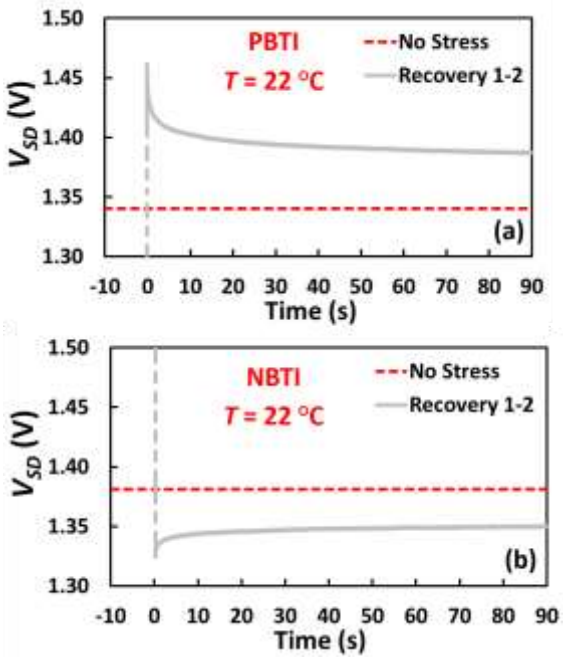

Fig. 6 Measured V_{SD} transient during the recovery transient after the first pulse. V_{GS}=0. (a) PBTI, (b) NBTI

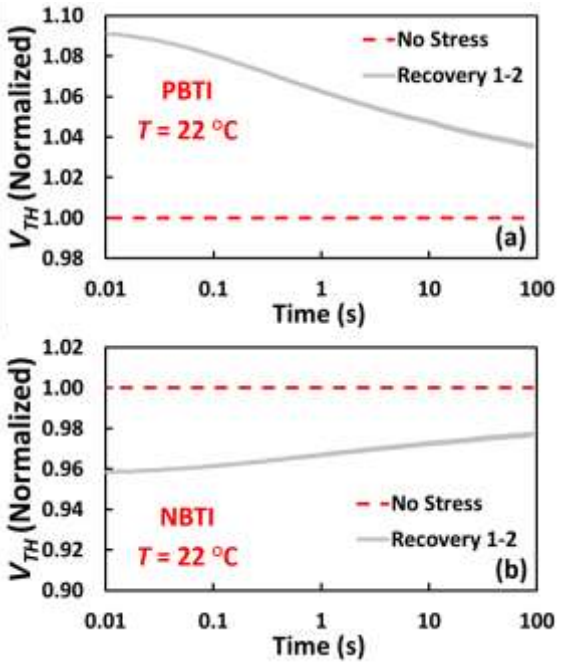

Fig. 7 Recovery of $V_{TH\text{-}NORMALIZED}$ after the stress pulse. (a) PBTI, (b) NBTI

A. *Long duration repetivitve stresses*

The impact of longer stress pulses and recovery times (in the range of minutes) was evaluated for both PBTI and NBTI stresses. The stress and characterization sequence is shown in Fig. 5(a) for the evaluation of PBTI and Fig. 5(b) for the evaluation of NBTI. The stress voltages are 22 V and -16 V for the PBTI and NBTI stresses respectively. The points where V_{SD} was measured for tracking the peak shift and recovery of V_{TH} after stress are identified from 0 (unstressed device) to 5 in Fig 5. The recovery transients (1-2) and (4-5) after each stress have been captured during 90 s.

The captured transient after the first pulse (1-2) is shown in Fig. 6(a) for the positive stress and Fig. 6(b) for the negative stress. As defined in the previous section and in more detail in [5], it is clearly observed how the positive stress shifts the measured V_{SD} upwards due to the increased V_{TH} and the negative gate stress shifts the measured V_{SD} downwards due to the reduction of V_{TH}.

The recovery of V_{SD}, thereby recovery of V_{TH}, after the stress after the first pulse is clearly observed in both cases. Using (1) the normalized V_{SD} value can be converted in the normalized V_{TH} value and the recovery of V_{TH} can be evaluated in more detail. This is shown in Fig 7 for both PBTI and NBTI stresses. For the device subjected to the positive stress the normalized increased of V_{TH} is higher, with an increase of around 9 %, than for the device subjected to negative stress, with a reduction of around 4 %.

The recovery is faster for the positive stress than for the negative stress and for both recovery transients there is an initial segment where the measured V_{SD} appears to be stationary. The authors attribute this to the transient response of the power supply during the change of conduction paths after the stress, when the voltage changes from low to high (PBTI) or high to low (NBTI).

The calculated V_{TH} shift for the points defined in Fig. 5 is presented in Fig. 8. For both PBTI and NBTI stresses, it is clearly observed how after 30 minutes recovery at V_{GS}=0, the

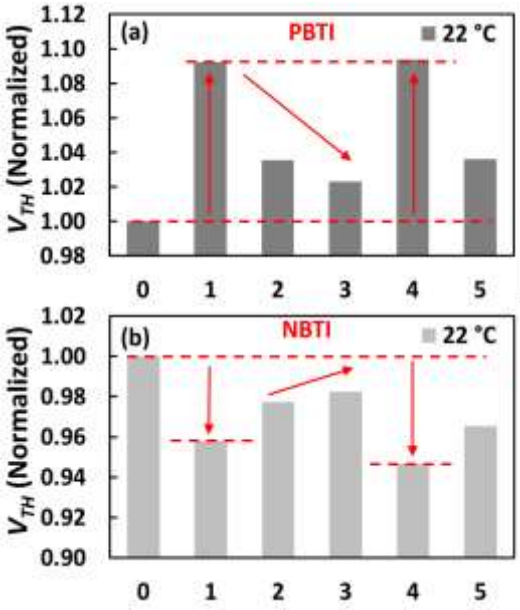

Fig. 8 Normalized V_{TH} shifts after cumulative pulsed stress tests (a) PBTI, (b) NBTI

threshold voltage recovers to a value close to the pre-stress V_{TH}, with the majority of the recovery happening in the first seconds after stress removal, as shown in the transient plots in Fig. 7. As mentioned in [3], this could have serious implications in the qualification of power devices. The impact of the cumulative stress of the second pulse is more apparent for the negative stress. After the first stress pulse, the initial peak shift detected for NBTI evaluation is around -4% whereas for the second pulse, the peak shift is approximately -5.5 %. For the positive stress despite the higher initial positive shift, the cumulative impact of the stresses is less apparent for the evaluated stress voltage. For both stress test, the device was attached to an aluminium block which acted as a heatsink and the impact of self-heating evaluated. In the case of NBTI, the temperature increase during the 15 minutes pulse was 1 °C, whereas in the case of PBTI, the impact of self-heating can be neglected.

B. *Short duration repetivitve stresses*

From the results presented in section III.A it is clearly observed how the shift of V_{TH} is more apparent for the first pulse and how it recovers exponentially after the stress removal. However, there is no information about the transient nature of the shift during the stress period. One of the main benefits of the presented characterization technique is that it will allow its evaluation using cumulative short stress pulses. This has been done for both negative and positive stresses in this paper. The stress time t_{STRESS} selected was 2 s, followed by a recovery time t_{REC} of 2 s at V_{GS}=0. The stresses were performed at the ambient temperature of 22 °C and the number of pulses was 40.

Fig. 9 shows the measured V_{SD} transient for V_{STRESS} voltages of 22 V and -26 V. In both cases, an initial shift of V_{SD} can be observed together with a partial recovery of V_{SD} during the relaxation time of 2 s. As described in the section II, this recovery represents the recovery of V_{TH} after the stress. Comparing Fig. 9(a) and Fig. 9(b), the rate of recovery is apparently higher for the positive stress, as the change of V_{SD} is higher during the recovery phase of the pulsed stress. Comparing both stresses, a continuous reduction of V_{SD} can be observed for the negative gate stress. Normalizing the peak V_{SD} value and the variation of V_{SD} during the recovery, for the PBTI stress a total peak shift of +7.4 % with a recovery of -4 % during the 2 s recovery phase are observed, whereas in the case of NBTI, the peak shift is -8.4 % with a relative recovery of + 1.5 %. In the case of the negative pulsed stresses a continuous reduction of V_{SD} can also be observed.

As BTI is also stress level dependent, another clear benefit of this method is that it allows to evaluate the impact on the V_{TH} shift of highly accelerated stress voltages for short periods of time and its impact on shift and recovery. The same pulsed stress tests of period 4 s was performed using a stress voltage of 35 V, well above the nominal gate voltage of the evaluated planar device and the results are shown in Fig. 10, for a temperature of 22 °C. As the results in Fig. 10 show, during the initial phase of the 35 V pulsed stress, there is an initial V_{SD} reduction indicating a reduction of V_{TH} followed by the expected increase of V_{SD} for PBTI

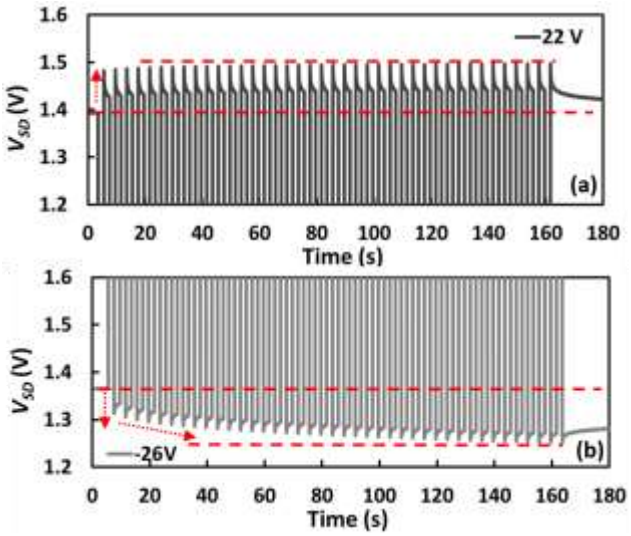

Fig. 9 (a) V_{SD} during PBTI pulsed stress tests. V_{STRESS}=22 V, V_{REC}=0 V, t_{STRESS}=2 s, t_{REC}=2 s. I_{SENSE}=50 mA, T=AMB
(b) V_{SD} during NBTI pulsed stress tests. V_{STRESS}=22 V, V_{REC}=0 V, t_{STRESS}=2 s, t_{REC}=2 s. I_{SENSE}=50 mA, T=AMB

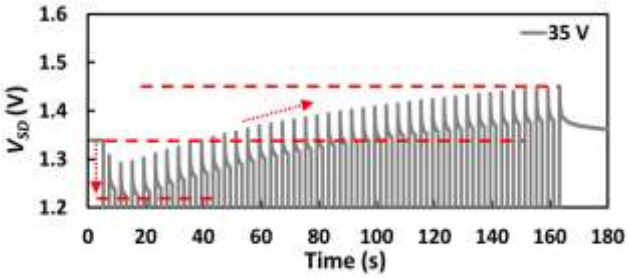

Fig. 10 V_{SD} during PBTI pulsed stress tests. V_{STRESS}=35 V, V_{REC}=0 V, t_{STRESS}=2 s, t_{REC}=2 s. I_{SENSE}=50 mA, T=AMB

during the final stage of the pulsed stress. This phenomenon of dip and rebound was already described in [7] for Si MOSFETs and is caused by the different contribution of the oxide trapped charges (decreasing V_{TH}) and the interface trapped charges (increasing V_{TH}) during the different stages of the stress. This is defined by (2) [7], where N_{ot} is the stress-induced change in the oxide trapped charge, *Nit* is stress-induced change in the interface trapped charge and C_{OX} is the specific gate oxide capacitance.

$$V_{TH} = V_{TH0} - \frac{qN_{ot}}{C_{OX}} + \frac{qN_{it}}{C_{OX}} \quad (2)$$

In a traditional long duration stress, this peculiar feature of the highly accelerated stress test would not be captured, hence the benefits of using the 3rd quadrant characteristics for assessing the impact of the BTI in SiC MOSFETs.

IV. Conclusion

In this paper it has been shown how the third quadrant characteristics of SiC MOSFETs can be used for evaluating the V_{TH} shift caused by BTI. It is shown how V_{SD} is and effective cursor for detecting the peak shift of V_{TH} and tracking the recovery of V_{TH} after the gate stress is removed. The implementation of this method is similar to the use of V_{SD} as TSEP. Using short duration pulsed stress tests, the phenomenon of dip and recovery of V_{TH} has been captured during initial stages of highly accelerated stress tests, hence demonstrating the importance that this methodology could have for characterizing BTI in SiC MOSFETs.

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